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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/650,670	08/29/2003	Takuma Hara	241984US2	7771

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EXAMINER

ROSE, KIESHA L

ART UNIT PAPER NUMBER

2822

DATE MAILED: 04/20/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No. 10/650,670	Applicant(s) HARA ET AL.	
	Examiner Kiesha L. Rose	Art Unit 2822	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 19 January 2005.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1-15 and 20-25 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☒ Claim(s) 12-15 is/are allowed.
- 6) ☒ Claim(s) 1-11 and 20-25 is/are rejected.
- 7) ☐ Claim(s) _____ is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☒ The drawing(s) filed on 29 August 2003 is/are: a) ☐ accepted or b) ☒ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☒ All b) ☐ Some * c) ☐ None of:
1. ☒ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. _____.
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- | | |
|--|---|
| 1) <input checked="" type="checkbox"/> Notice of References Cited (PTO-892) | 4) <input type="checkbox"/> Interview Summary (PTO-413)
Paper No(s)/Mail Date. _____ |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948) | 5) <input type="checkbox"/> Notice of Informal Patent Application (PTO-152) |
| 3) <input type="checkbox"/> Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)
Paper No(s)/Mail Date _____ | 6) <input type="checkbox"/> Other: _____ |

DETAILED ACTION

This Office Action is in response to the amendment filed 19 January 2005.

Drawings

Figure 23 should be designated by a legend such as --Prior Art-- because only that which is old is illustrated. See MPEP § 608.02(g). Corrected drawings in compliance with 37 CFR 1.121(d) are required in reply to the Office action to avoid abandonment of the application. The replacement sheet(s) should be labeled "Replacement Sheet" in the page header (as per 37 CFR 1.84(c)) so as not to obstruct any portion of the drawing figures. If the changes are not accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

Claim Rejections - 35 USC § 112

The following is a quotation of the second paragraph of 35 U.S.C. 112:

The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

Claim 22 is rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention. Claim 22 discloses a fourth semiconductor region of a second conductivity type provided on the "fourth semiconductor region". It is unclear how the fourth region is formed on the fourth region.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 1-4, 6 and 8 are rejected under 35 U.S.C. 102(b) as being anticipated by Ohzu et al. (U.S. Patent 5,378,914).

Ohzu discloses a semiconductor device (Fig. 5a) that contains a first main electrode (60), second main electrode (61), a semiconductor base region (202) of a first conductivity type, a gate electrode (55) provided in a trench through an insulating film (54) and the trench penetrating the semiconductor base region, a first semiconductor region (203) of second conductivity type provided under the semiconductor base region and a second semiconductor region (57) of a first conductivity type provided under the first semiconductor region, wherein the second semiconductor region is in contact with the trench and the bottom of the trench is provided in the second semiconductor region and is spaced apart from the trench, a flow of current between the first and second main electrodes when a voltage of a predetermined direction is applied between the electrodes being controllable with a voltage applied to the gate electrode and a depleted region extending from a junction between the first and second semiconductor regions reaching the trench.

In regards to claim 8,

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A first semiconductor region (57) of a second conductivity type; a second semiconductor region (56) of a first conductivity type provided on the first semiconductor region, a third semiconductor region (51) of a second conductivity type provided on the second semiconductor region, a fourth semiconductor region (52) of a first conductivity type provided on the third semiconductor region, a fifth semiconductor region (53) of a second conductivity type provided on the fourth semiconductor region, a trench (55) penetrating at least the third through fifth semiconductor regions, a bottom of the trench being provided within the second semiconductor region; and a gate electrode (55) provided in the trench through an insulating film (54).

(e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

Claims 8-11 are rejected under 35 U.S.C. 102(e) as being anticipated by Onishi et al. (U.S. Patent 6,621,132).

Onishi discloses a semiconductor device (Fig. 3) that contains a first semiconductor region (39) of a second conductivity type; a semiconductor layer provided on the first semiconductor region and having a plurality of second semiconductor regions (31a) of a first conductivity type and a plurality of third semiconductor regions (31b) of a second conductivity type, the second and the third semiconductor regions being arranged alternately along with two diagonal directions on the first semiconductor region; a fourth semiconductor region (32), a fifth semiconductor

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region (32d) of a second conductivity type provided on the fourth semiconductor region, a trench (34) penetrating at least the third through the fifth semiconductor regions, a bottom of the trench being provided within the semiconductor layer; and a gate electrode provided in the trench through an insulating film and the second and third regions are depleted. The concentration of the second and third region is $3.0 \times 10^{15} \text{cm}^3$. (Column 6, lines 32-36)

Claims 20-23, as far as understood, are rejected under 35 U.S.C. 102(e) as being anticipated by Onishi et al. (U.S. Patent 6,621,132).

Onishi discloses a semiconductor device (Fig. 3) that contains a first semiconductor region (39) of a second conductivity type; a semiconductor layer provided on the first semiconductor region and having a plurality of second semiconductor regions (31a) of a first conductivity type and a plurality of third semiconductor regions (31b) of a second conductivity type, the second and the third semiconductor regions being arranged alternately along with two diagonal directions on the first semiconductor region; a fourth semiconductor region (32d), a fifth semiconductor region (32) of a second conductivity type provided on the fourth semiconductor region, a trench (34) penetrating at least the fourth and the fifth semiconductor regions, a bottom of the trench being provided within the semiconductor layer; and a gate electrode provided in the trench through an insulating film. The concentration of the second and third region is $3.0 \times 10^{15} \text{cm}^3$. (Column 6, lines 32-36)

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

Claims 5 and 7 are rejected under 35 U.S.C. 103(a) as being unpatentable over Ohzu in view of Onishi.

Ohzu discloses all the limitations except for a plurality of first and second semiconductor regions or the first and second semiconductor regions arranged in an alternating arrangement. Whereas Onishi discloses a semiconductor device (Fig. 3) that contains a semiconductor base region (32d) of first conductivity type, a plurality of first semiconductor regions (31b) of a second conductivity type and a plurality of third semiconductor regions (31a) of a first conductivity type, the second and the third semiconductor regions being arranged alternately and perpendicular to the depth direction of the trench. The first and second semiconductor regions are formed of first and second conductivity types in an alternating arrangement to increase switching speed, reduce on-resistance and to have a high breakdown voltage. (Abstract, Column 1, line 67 and Column 2, lines 1-2) Therefore it would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the device of Ohzu by incorporating a plurality of first and second semiconductor regions and have them in an alternating arrangement to increase switching speed, reduce on-resistance and to have a high breakdown voltage as taught by Onishi.

Allowable Subject Matter

Claims 12-15 are allowed.

The following is an examiner's statement of reasons for allowance: Claims 12-15 are allowable because prior art does not show alone or in combination along with the limitations of the independent claims such as a sixth semiconductor region of second conductivity type provided in contact with the bottom of the trench.

Any comments considered necessary by applicant must be submitted no later than the payment of the issue fee and, to avoid processing delays, should preferably accompany the issue fee. Such submissions should be clearly labeled "Comments on Statement of Reasons for Allowance."

Response to Arguments

Applicant's arguments with respect to claims 1-15 and 20-25 have been considered but are moot in view of the new ground(s) of rejection.

Conclusion


Any inquiry concerning this communication or earlier communications from the examiner should be directed to Kiesha L. Rose whose telephone number is 571-272-1844. The examiner can normally be reached on M-F 8:30-6:00 off 2nd Mondays.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Amir Zarabian can be reached on 571-272-1852. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

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Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

KLR


Michael Trinh
Primary Examiner

Act SPE